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UTILITY PATENT APPLICATION TRANSMITTAL

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First Named Inventor or Application Identifier:	NAYLER
Title: Arrangement for Reducing Transmitted Jitter	

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:
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Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form
2. [X] Specification, Claims & Abstract ..... [Total Pages: 13]
3. [X] Formal Drawing(s) *(35 USC 113)* .... [Total Sheets: 7]
4. [X] Oath or Declaration ..... [Total Pages: 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation by Reference (usable if Box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [X] Microfiche Computer Program *(Appendix)* [Total Pages: 3]
7. [ ] Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, status still proper and desired.
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [X] Other: Claim of Priority

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: ____/____

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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For: ARRANGEMENT FOR REDUCING TRANSMITTED JITTER

CLAIM OF PRIORITY

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Applicant hereby claims priority under 35 U.S.C. 119 for the benefit of the filing date of the Provisional Application No. 60/218,571, filed July 13, 2000.

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E0954 / 95-346

ARRANGEMENT FOR REDUCING TRANSMITTED JITTER

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to pulse position modulation communications systems, for example home networking physical layer transceivers.

BACKGROUND ART

Local area networks use a network cable or other media to link stations on the network. Each local area network architecture uses a media access control (MAC) enabling network interface cards at each station to share access to the media.

Conventional local area network architectures use a media access controller operating according to half-duplex or full duplex Ethernet (ANSI/IEEE standard 802.3) protocol using a prescribed network medium, such as 10BaseT. Newer operating systems require that a network station be able to detect the presence of the network. In an Ethernet 10BaseT environment, the network is detected by the transmission of a link pulse by the physical layer (PHY) transceiver. The periodic link pulse on the 10BaseT media is detected by a PHY receiver, which determines the presence of another network station transmitting on the network medium based on detection of the periodic link pulses. Hence, a PHY transceiver at station A is able to detect the presence of station B, without the transmission or reception of data packets, by the reception of link pulses on the 10BaseT medium from the PHY transmitter at station B.

Chipsets have being developed that enable computers to be linked together using conventional twisted pair telephone lines instead of established local area network media such as 10BaseT. Such chipsets, implemented according to the Home Phoneline Networking Alliance (HomePNA) Specification 2.0, provide the advantage that existing telephone wiring in a home may be used to implement a home network environment. However, telephone lines are inherently noisy due to spurious noise caused by electrical devices in the home, for example dimmer switches, transformers of home appliances, etc. In addition, the twisted pair telephone lines suffer from turn-on transients due to on-hook and off-hook and noise pulses from the standard POTS telephones, and electrical systems such as heating and air-conditioning systems, etc.

An additional problem in implementing home networks according to the HomePNA specification 2.0 is that the HomePNA specification specifies pulse transmission times relative to a prescribed multiple of reference clock cycles. Specifically, the HomePNA specification defines a TIC

time as seven (7) counts of a 60 MHz clock, resulting in a TIC time having a duration of 116.667 nanoseconds: hence, the HomePNA specification requires HomePNA pulses to be transmitted on the boundaries of the 166.667ns TIC times.

Although the TIC time can be readily generated in a HomePNA transmitter using a divide by seven counter driven by a 60 MHz clock, implementation of the acquired TIC time becomes more difficult if a 60 MHz clock is not readily available, or if a designer prefers not to use a 60 MHz oscillator. For example, existing logic within the physical layer transceiver may utilize different clock speeds requiring a difference the oscillator, such as a 32 MHz clock. In such case, the use of both a 32 MHz based oscillator and a 60 MHz based oscillator may undesirably result in an expensive transceiver.

Attempts to utilize a 32 MHz clock for generation of the 7/60MHz TIC times, however, results in jitter due to the face differences between the specified transmit clock (e.g., 7/60MHz) and the actual transmit clock (e.g., 32 MHz). Hence, the use of an alternative transmit clock may introduce jitter that adversely affects the required low error data rate transmission.

SUMMARY OF THE INVENTION

There is a need for an arrangement that minimizes jitter in transmit waveform communications systems that use a single transmit clock, separate from a specified transmit clock.

There also is a need for an arrangement in a digital transmission system that compensates for phase errors based on frequency differences between a transmit clock utilized by the digital transmission system and a prescribed transmit frequency.

These and other needs are attained by the present invention, where a system such as a pulse transmitter includes a phase correction module configured for detecting a phase error between a transmit clock and a prescribed clock specification at a transmit clock instance. The transmit clock instance represents an instance in time in which the pulse transmitter is to transmit data according to the prescribed clock specification. The pulse transmitter also includes pulse shape tables, each configured for outputting a corresponding waveform sample set of a prescribed waveform relative to a corresponding phase offset. Hence, the pulse transmitter is able to compensate for phase differences between the transmit clock utilized by the pulse transmitter and the prescribed clock specification, by outputting a selected waveform sample set that has a corresponding phase offset that compensates for the detected phase error, optimizing the performance of pulse position modulation communications systems that are adversely affected by transmit jitter.

One aspect of the present invention provides a method in a transmission system configured for outputting a set of waveform samples starting at a transmission time instant according to a transmit clock. The method includes determining a phase error between the transmit clock and a prescribed

transmit clock relative to the transmission time instant. The method also includes outputting a selected waveform sample set based on the determined phase error, the waveform sample set having samples of a prescribed waveform relative to a corresponding phase offset, the phase offset of the selected waveform sample set correcting for the determined phase error. Determination of the phase error between the transmit clock and the prescribed transmit clock relative to the transmission time instant enables the transmission system to compensate for the detected phase error, improving the transmission performance of the transmitted waveform to minimize jitter. Moreover, the selection of a waveform sample set having samples of a prescribed waveform relative to a corresponding phase offset enables the precise correction of the determined phase error with minimal complexity.

Another aspect of the present invention provides a transmission system configured for outputting a set of waveform samples starting at a transmission time instant according to a transmit clock. The system includes a pulse shape table circuit configured for outputting a selected waveform sample set of a prescribed waveform relative to a selected phase offset in response to an address signal and a selection signal. The system also includes a phase correction module configured for determining a phase error between the transmit clock and a prescribed transmit clock relative to the transmission time instant, the phase correction module outputting the address signal and the selection signal at the transmission time instant for output of the selected waveform sample set correcting for the determined phase error.

Additional advantages and novel features of the invention will be set forth in part in the description which follows and in part will become apparent to those skilled in the art upon examination of the following or may be learned by practice of the invention. The advantages of the present invention may be realized and attained by means of instrumentalities and combinations particularly pointed in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference is made to the attached drawings, wherein elements having the same reference numeral designations represent like elements throughout and wherein:

Figure 1 is a block diagram illustrating a pulse position transmitter having a phase correction system for correcting for determined phase errors between a transmit clock and a prescribed transmit clock according to an embodiment of the present invention.

Figures 2A and 2B are diagrams illustrating samples of a prescribed transmit pulse waveform generated by the pulse position transmitter of Figure 1.

Figure 3 is a diagram illustrating available phase offsets for the pulse shape tables of Figure 1.

Figure 4 is a diagram illustrating in detail the phase correction module of Figure 1.

Figure 5 is a diagram illustrating the table select logic of Figure 4.

Figure 6 is a diagram illustrating the relative difference between the transmit clock and a prescribed transmit clock.

Figure 7 is a diagram illustrating differences between an uncorrected analog output pulse and a corrected analog output pulse generated based on a waveform sample set having a corresponding phase offset from the phase correction system of Figure 1.

BEST MODE FOR CARRYING OUT THE INVENTION

Figure 1 is a block diagram illustrating a pulse position modulation communications system 10 configured for outputting an analog pulse waveform at selected transmission time instances according to an embodiment of the present invention. The pulse position modulation communications system 10 may be implemented, for example, in a home PNA physical layer transmitter configured for generating analog home PNA pulses on the boundaries of TIC times that are defined based on a specified transmit clock having a normalized period of 7/60. In particular, the pulse position modulation communications system 10 includes a coding block 12 configured for generating time interval values, representing respective data values, as unit multiples of a 166.667ns TIC time.

The system 10 also includes a phase correction module 14, and a pulse shape table circuit 15. The pulse shape table circuit 15 includes pulse shape tables 16 and a multiplexer 18. The multiplexer 18 is configured for outputting a selected waveform sample set that corrects for determined phase errors between transmission time instances specified by the time interval values from the coding block 12, and a 32 MHz transmit clock 24.

Figures 2A and 2B are diagrams illustrating the waveform samples of a prescribed transmit waveform 32, where Figure 2B illustrates the transmit waveform 32 in further detail at a peak 32a. Figures 2A and 2B are used to illustrate the pulse shape where specified transmission times are given in multiples of a clock with normalized period 7/60, and the actual transmission clock normalized period is 1/32. The sample values 30 are plotted against a normalized timescale with a minimum sample spacing of 1/480 = 1/(15*32). The minimum sample spacing is determined based on the lowest common denominator between the different normalized clock periods 1/32 and 1/60. Hence, the number of pulse shape tables 16 corresponds to the number of possible phases 34 of the specified clock (7/60) relative to the transmit clock 24.

Each pulse shape table 16 is configured for outputting a corresponding waveform sample set 30, illustrated in Figures 2A and 2B, of a prescribed transmit waveform 32 relative to a corresponding phase offset 34, illustrated in Figure 3. In particular, each table 16 is configured for storing equal time spaced waveform samples 30 starting with a corresponding delay time 34. For example, the pulse shape table 16_0 would store thirty-two (32) waveform samples of the waveform sample set 30a representing samples of

the transmit waveform 32 with the phase/time offset 34_0, and the pulse shape table 16_9 (not shown) would store thirty-two (32) waveform samples of the waveform sample set 30b representing samples of the transmit waveform 32 with the phase/time offset 34_9. Hence, each pulse shape table 16 stores waveform samples having a normalized period spacing of 1/32.

The phase correction module 14 retrieves from the coding block 12 the time interval values representing transmit data as integer multiples of the normalized period 7/60 (i.e., "TIC times"), and determines a transmission time instant (i.e., the instant in time at which the waveform is to be output by the pulse position modulation communications system 10) for the prescribed waveform 32 relative to a start of frame. The phase correction module 14 also determines the phase error between the 32 MHz transmit clock 24 and the prescribed transmit clock having the normalized period of 7/60 at the transmission time instant. The phase correction module 14 then selects samples 30 of the specified transmit pulse shape 32 that correct for the determined phase error between the 32 MHz clock and the prescribed 7/60 transmit clock at the transmission time instant by outputting to the multiplexer 18 a Table Select signal having a value based on the determined phase error, and outputting to the pulse shape tables 16 a sequence of Table Address signals starting at the transmission time instant; hence, the analog pulse waveform output after analog reconstruction by the digital to analog converter (DAC) 20 and filtering by the low pass filter 22 is a signal having substantially zero phase noise relative to the prescribed transmit clock. Hence, the phase correction module 14 can correct for detected phase errors between the actual 32 MHz transmit clock 24 in the prescribed 7/60 transmit clock, even when the actual transmit clock is not a simple frequency multiple of the prescribed transmit clock.

Figure 4 is a block diagram illustrating in detail the phase correction module 14 of Figure 1 according to an embodiment of the present invention. The phase correction module 14 includes a coding interface controller 40 configured for obtaining the time interval specifications from the coding block 12, relative to a start of frame signal received, for example, from an IEEE 802.3 based media access controller (not shown). In particular, the coding interface controller 40 obtains the successive time intervals, represented as integer multiples of TIC times, from the coding block 12.

The phase correction module 14 also includes an accumulator block 42, having an adder 44 and a register 46, and configured for determining the transmission time instant based on the obtained time intervals. In particular, the adder 44 adds the obtained integer value to previously accumulated integer values stored in the register 46 to obtain an accumulated integer. The register 46 is continually updated with the accumulated integer until cleared by the start of frame signal. Hence, the register 46 stores the next transmission time instant as an integer number of TIC times following the start of frame signal.

The phase correction module 14 also includes a multiplier 48 for calculating the transmission time instant as a specified time by multiplying the accumulated integer stored in the register 46 with a normalized value of the prescribed transmit clock, namely the normalized period 7/60. Hence, the

specified time represents the transmission time instant within the domain of the specified 7/60 transmission clock.

The phase correction module 14 also includes a modulo counter 50 configured for counting through the number of available time offsets 34 each cycle of the 32 MHz clock 24 relative to the start of frame signal. The phase correction module 14 also includes a transmit clock incidence detector 52, and table select logic 54. The transmit clock incidence detector 52 includes a register 56, an adder 58, an adder 60, a comparator 62, and a sequencer 64. The register 56 is configured for storing accumulated values, calculated by the adder 58, of time intervals according to the normalized period 1/32 and based on the 32 MHz transmit clock. Hence, the register 56 outputs the actual elapsed time from the start of frame signal according to the normalized period 1/32 relative to the 32 MHz clock 24.

The adder 60 outputs the difference between the actual time (measured based on the normalized period 1/32 based on the 32 MHz transmit clock) and the specified transmit time (based on the normalized period 7/60 of the specified transmit clock), to the comparator 62, which outputs an output incidence signal when the difference output by the adder 60 is within the prescribed phase offset resolution of 1/32, defined by the normalized period 1/32. Hence, the comparator 62 outputs the output incidence signal to the table address sequencer 64 to identify an output incidence where the actual counted time relative to the 32 MHz transmit clock 24 coincides with the transmission time instant (i.e., the specified time) within the prescribed phase offset resolution based on the normalized period 1/32. The table address sequencer 64, in response to reception of the output incidence signal, begins outputting the sequence of table address signals (i.e., the sequence of address values 0, 1, 2, ... 31) based on the 32 MHz clock signal 24 to coincide with one of the offset signals 34 of Figure 3.

Hence, the modulo counter 50 counts through one of the 15 possible modulo counter values each cycle of the 32 MHz transmit clock 24, representing the 15 possible phase offsets within the transmit clock cycle relative to the start of frame. The transmit clock incidence detector 52 detects the actual output incidence at which point the actual counted time relative to the transmit clock coincides with the transmission time instant within the waveform sample resolution. Hence, the phase correction module 14 uses the modulo counter value at the time the initiation of outputting the sequence of table address signals to identify the phase error between the transmit clock and the prescribed transmit clock relative to the transmission time instant.

The phase correction module 14 also includes table select logic 54, illustrated in detail in Figure 5. The table select logic 54 includes a comparator 70 and multiplexers 72 and 74. The table select logic is configured for outputting the table select signal by selectively offsetting the modulo account value based on whether the accumulated integer value of the TIC time position is an even number or an odd number relative to the normalized multiple of the prescribed transmit clock. If the accumulated integer value is an even number (i.e., bit 0 equals 0), the multiplexer 72 outputs the modulo account value as the table select value to the multiplexer 18. However if the accumulated integer value is an odd number (i.e., bit 0 equals

1), the table select logic 54 offsets the modulo count based on whether the accumulated value is less than 7.5 or greater than 7.5. If the accumulated integer value is an odd number that is less than 7.5, a value of 8 is added to the modulo count, else if the accumulated integer value is an odd number that is greater than 7.5, the value of 8 is subtracted from the modulo count. Hence, the table select logic 54 corrects for computation of TIC numbers having an odd value, illustrated with respect to Figure 6 relative to the 32 MHz clock and the specified 30 MHz clock.

Hence, the phase correction module 14 is able to determine a phase error between the transmit clock and a prescribed transmit clock relative to the transmission time instant. The phase correction module 14 outputs the sequence of table address signals to the pulse shape tables 16, and the table selection signal to the multiplexer 18 to determine the phase error at the transmission time instant. The multiplexer 18 outputs the waveform samples for the selected pulse shape table to the DAC 20, enabling the output waveform to correct for the detected phase error. For example, Figure 7 is a diagram illustrating the simulated output of the analog low pass filter 22. The lightly shaded lines 80 illustrate the overlay of 15 output pulses being transmitted at multiples of the specified TIC time when only one pulse shaping table is used synchronous to the actual transmission (1/32) clock. The dark lines 82 illustrate the overlay of 15 output pulses being transmitted at multiples of the specified TIC time when 15 different pulse shaping tables are used as selected by the phase correction module 14, illustrating a significant reduction in jitter. In addition, the attached appendix illustrates a simulation program on page 1 and the results on pages 2 and 3. As shown in the results on pages 2 and 3 of the appendix, the integer TIC multiples create noninteger time offsets relative to the 1/32 transmit clock, however the phase offset can be precisely corrected by integer-based selection of one of the 15 available waveforms from the respective pulse shape tables 16.

According to the disclosed embodiment, jitter can be substantially reduced in pulse position modulation communication systems by selecting appropriate samples of the specified pulse shape that compensate for detected phase differences between a specified transmit clock and the actual transmit clock. Moreover, the reduction in jitter can be implemented with minimal complexity, eliminating the necessity for more complex feedback systems.

Although the disclosed embodiment utilizes multiple pulse shape tables and a multiplexer for retrieval of the waveform samples having the proper phase offset for correcting the determined phase error, the phase shape table circuit 15 could be implemented as a single memory having multiple stored waveform samples in respective memory segments, where the selection signal is used for the most significant bits of an address signal to address a selected memory segment, and the address signals are used for the least significant bits of the address signal to sequentially address the waveform samples from the selected memory segment. The pulse shape table circuit 15 could also be implemented using a single pulse shape table 16 and an interpolator that interpolates the waveform samples based on the determined phase error.

While this invention has been described with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is Claimed Is:

1. A method in a transmission system configured for outputting a set of waveform samples starting at a transmission time instant according to a transmit clock, the method comprising:

determining a phase error between the transmit clock and a prescribed transmit clock relative to the transmission time instant; and

outputting a selected waveform sample set based on the determined phase error, the waveform sample set having samples of a prescribed waveform relative to a corresponding phase offset, the phase offset of the selected waveform sample set correcting for the determined phase error.

2. The method of claim 1, further comprising:

obtaining a first time interval specification relative to a start of frame signal for a data frame to be transmitted; and

determining the transmission time instant based on the first time interval specification and the start of frame signal.

3. The method of claim 2, wherein the step of obtaining the first time interval specification includes generating a request, to a coding block, for the first time interval specification.

4. The method of claim 2, wherein the step of determining the transmission time instant includes adding the first time interval specification to prior time interval specifications received following the start of frame signal to obtain an accumulated integer.

5. The method of claim 4, wherein the step of determining the transmission time instant includes calculating the transmission time instant by multiplying the accumulated integer by a normalized value of the prescribed transmit clock.

6. The method of claim 5, wherein the step of determining a phase error includes:

incrementing a modulo counter according to the transmit clock and based on the start of frame signal, the modulo counter outputting a modulo count having a number of possible values based on a corresponding number of different phase values between the prescribed transmit clock and the transmit clock, each possible value identifying a corresponding one of a plurality of the waveform sample sets having a corresponding phase offset; and

identifying an output incidence where an actual counted time relative to the transmit clock coincides with the transmission time instant within a prescribed phase offset resolution.

7. The method of claim 6, wherein the outputting step includes selecting the selected one waveform sample set based on the modulo count value at the output incidence.

8. The method of claim 7, wherein the selecting step includes selecting the selected one waveform sample using one of the modulo count value and an offset value of the modulo count value based on whether the accumulated integer is an even number or an odd number.

9. The method of claim 2, wherein the step of determining a phase error includes:

incrementing a modulo counter according to the transmit clock and based on the start of frame signal, the modulo counter outputting a modulo count having a number of possible values based on a corresponding number of different phase values between the prescribed transmit clock and the transmit clock, each possible value identifying a corresponding one of a plurality of the waveform sample sets having a corresponding phase offset; and

identifying an output incidence where an actual counted time relative to the transmit clock coincides with the transmission time instant within a prescribed phase offset resolution.

10. The method of claim 9, wherein the outputting step includes selecting the selected one waveform sample set based on the modulo count value at the output incidence.

11. The method of claim 10, wherein the selecting step includes selecting the selected one waveform sample by outputting to a multiplexer one of the modulo count value and an offset value of the modulo count value, based on whether the transmission time instant is an even number or an odd number relative to a normalized multiple of the transmit clock.

12. A transmission system configured for outputting a set of waveform samples starting at a transmission time instant according to a transmit clock, the system comprising:

a pulse shape table circuit configured for outputting a selected waveform sample set of a prescribed waveform relative to a selected phase offset in response to an address signal and a selection signal; and

a phase correction module configured for determining a phase error between the transmit clock and a prescribed transmit clock relative to the transmission time instant, the phase correction module outputting the address signal and the selection signal at the transmission time instant for output of the selected waveform sample set correcting for the determined phase error.

13. The system of claim 12, wherein the phase correction module includes:

a coding interface controller configured for obtaining a first time interval specification relative to a start of frame signal for a data frame to be transmitted; and

an accumulator block configured for determining the transmission time instant based on adding the first time interval specification to a previously accumulated integer relative to the start of frame signal to obtain an accumulated integer, and based on an accumulate signal output by the coding interface controller.

14. The system of claim 13, wherein the phase correction module further includes a multiplier for calculating the transmission time instant by multiplying the accumulated integer with a normalized value of the prescribed transmit clock.

15. The system of claim 12, wherein the phase correction module includes:

a modulo counter configured for modulo counting, as a modulo count, the selection signal each cycle of the transmit clock and based on a start of frame signal, the modulo count having a number of possible values based on a corresponding number of different phase values between the prescribed transmit clock and the transmit clock; and

a transmit clock incidence detector configured for identifying an output incidence where an actual counted time relative to the transmit clock coincides with the transmission time instant within a prescribed phase offset resolution, the transmit clock incidence detector configured for outputting the address signal at the identified output incidence.

16. The system of claim 15, wherein the phase correction module further includes table select logic configured for outputting the selection signal by selectively offsetting the modulo count based on whether the transmission time instant is an even number or an odd number relative to a normalized multiple of the prescribed transmit clock.

17. The system of claim 12, wherein the pulse shape table circuit includes:

a plurality of pulse shape tables, each configured for outputting the corresponding waveform sample set of the prescribed waveform relative to a corresponding phase offset in response to the address signal; and

a multiplexer configured for outputting from a selected one of the pulse shape tables the corresponding selected waveform sample set in response to the selection signal.

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ARRANGEMENT FOR REDUCING TRANSMITTED JITTER

ABSTRACT OF THE DISCLOSURE

A pulse transmitter includes a phase correction module configured for detecting a phase error between a transmit clock and a prescribed clock specification at a transmit clock instance. The transmit clock instance represents an instance in time in which the pulse transmitter is to transmit data according to the prescribed clock specification. The pulse transmitter also includes pulse shape tables, each configured for outputting a corresponding waveform sample set of a prescribed waveform relative to a corresponding phase offset. Hence, the pulse transmitter is able to compensate for phase differences between the transmit clock utilized by the pulse transmitter and the prescribed clock specification, by outputting a selected waveform sample set that has a corresponding phase offset that compensates for the detected phase error, optimizing the performance of pulse position modulation communications systems that are adversely affected by transmit jitter.

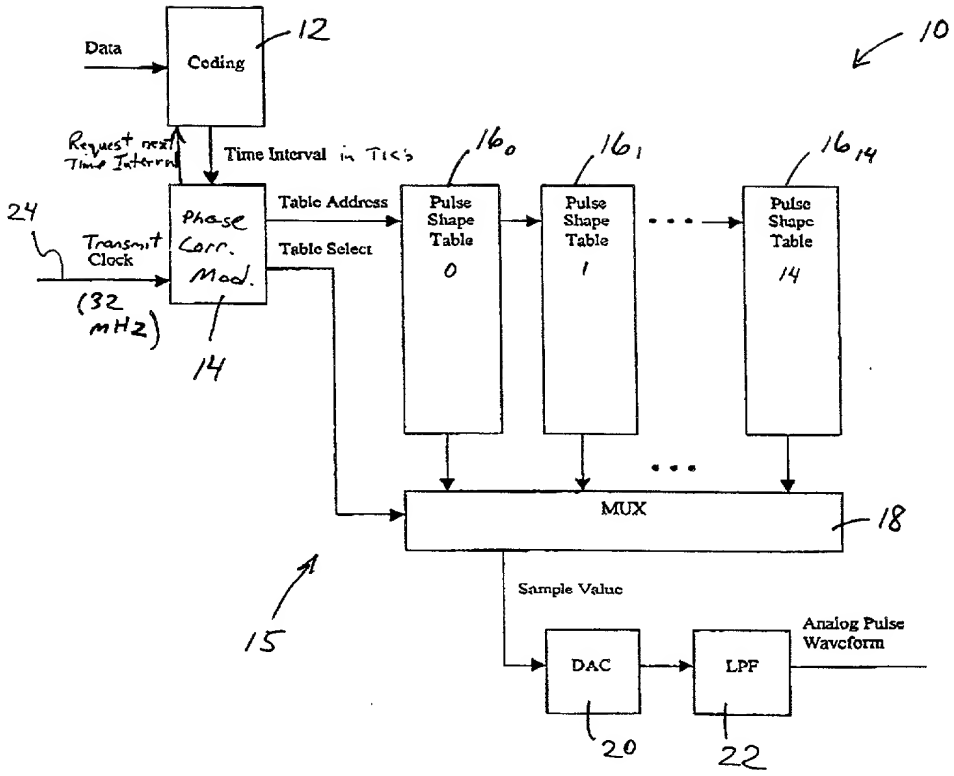
```
T60=1/60;
tic=7*T60;
T32=1/32;
tnum = 128;
TIC = 1:1:tnum;
ttime = TIC*tic./T32;
ttmod16 = mod(floor(TIC*tic./T32),16);
toffset = (TIC*tic./T32)*T32 - (floor(TIC*tic./T32)*T32);
phase = round(toffset./(T32/15));

for n=1:tnum
   if mod(n,2)==0
      calcphase(n) = phase(n);
   else
      if ttmod16(n)<7.5
         calcphase(n) = ttmod16(n)+8;
      else
         calcphase(n) = ttmod16(n)-8;
      end
   end
end

table= [TIC' ttime' ttmod16' toffset' phase' calcphase'];
```

Table = TIC No.	No. of T32 Clocks	No. of Whole T32 Clocks	Tim'g Offset relative to T32 Clock	Phase = (offset/T32)*15	Table Select from Algorithm
1.0000	3.7333	3.0000	0.0229	11.0000	11.0000
2.0000	7.4667	7.0000	0.0146	7.0000	7.0000
3.0000	11.2000	11.0000	0.0062	3.0000	3.0000
4.0000	14.9333	14.0000	0.0292	14.0000	14.0000
5.0000	18.6667	2.0000	0.0208	10.0000	10.0000
6.0000	22.4000	6.0000	0.0125	6.0000	6.0000
7.0000	26.1333	10.0000	0.0042	2.0000	2.0000
8.0000	29.8667	13.0000	0.0271	13.0000	13.0000
9.0000	33.6000	1.0000	0.0188	9.0000	9.0000
10.0000	37.3333	5.0000	0.0104	5.0000	5.0000
11.0000	41.0667	9.0000	0.0021	1.0000	1.0000
12.0000	44.8000	12.0000	0.0250	12.0000	12.0000
13.0000	48.5333	0	0.0167	8.0000	8.0000
14.0000	52.2667	4.0000	0.0083	4.0000	4.0000
15.0000	56.0000	8.0000	0	0	0
16.0000	59.7333	11.0000	0.0229	11.0000	11.0000
17.0000	63.4667	15.0000	0.0146	7.0000	7.0000
18.0000	67.2000	3.0000	0.0063	3.0000	3.0000
19.0000	70.9333	6.0000	0.0292	14.0000	14.0000
20.0000	74.6667	10.0000	0.0208	10.0000	10.0000
21.0000	78.4000	14.0000	0.0125	6.0000	6.0000
22.0000	82.1333	2.0000	0.0042	2.0000	2.0000
23.0000	85.8667	5.0000	0.0271	13.0000	13.0000
24.0000	89.6000	9.0000	0.0187	9.0000	9.0000
25.0000	93.3333	13.0000	0.0104	5.0000	5.0000
26.0000	97.0667	1.0000	0.0021	1.0000	1.0000
27.0000	100.8000	4.0000	0.0250	12.0000	12.0000
28.0000	104.5333	8.0000	0.0167	8.0000	8.0000
29.0000	108.2667	12.0000	0.0083	4.0000	4.0000
30.0000	112.0000	0	0	0	0
31.0000	115.7333	3.0000	0.0229	11.0000	11.0000
32.0000	119.4667	7.0000	0.0146	7.0000	7.0000
33.0000	123.2000	11.0000	0.0063	3.0000	3.0000
34.0000	126.9333	14.0000	0.0292	14.0000	14.0000
35.0000	130.6667	2.0000	0.0208	10.0000	10.0000
36.0000	134.4000	6.0000	0.0125	6.0000	6.0000
37.0000	138.1333	10.0000	0.0042	2.0000	2.0000
38.0000	141.8667	13.0000	0.0271	13.0000	13.0000
39.0000	145.6000	1.0000	0.0187	9.0000	9.0000
40.0000	149.3333	5.0000	0.0104	5.0000	5.0000
41.0000	153.0667	9.0000	0.0021	1.0000	1.0000
42.0000	156.8000	12.0000	0.0250	12.0000	12.0000
43.0000	160.5333	0	0.0167	8.0000	8.0000
44.0000	164.2667	4.0000	0.0083	4.0000	4.0000
45.0000	168.0000	8.0000	0	0	0
46.0000	171.7333	11.0000	0.0229	11.0000	11.0000
47.0000	175.4667	15.0000	0.0146	7.0000	7.0000
48.0000	179.2000	3.0000	0.0062	3.0000	3.0000
49.0000	182.9333	6.0000	0.0292	14.0000	14.0000
50.0000	186.6667	10.0000	0.0208	10.0000	10.0000
51.0000	190.4000	14.0000	0.0125	6.0000	6.0000
52.0000	194.1333	2.0000	0.0042	2.0000	2.0000
53.0000	197.8667	5.0000	0.0271	13.0000	13.0000
54.0000	201.6000	9.0000	0.0187	9.0000	9.0000
55.0000	205.3333	13.0000	0.0104	5.0000	5.0000
56.0000	209.0667	1.0000	0.0021	1.0000	1.0000
57.0000	212.8000	4.0000	0.0250	12.0000	12.0000
58.0000	216.5333	8.0000	0.0167	8.0000	8.0000
59.0000	220.2667	12.0000	0.0083	4.0000	4.0000
60.0000	224.0000	0	0	0	0
61.0000	227.7333	3.0000	0.0229	11.0000	11.0000
62.0000	231.4667	7.0000	0.0146	7.0000	7.0000
63.0000	235.2000	11.0000	0.0063	3.0000	3.0000
64.0000	238.9333	14.0000	0.0292	14.0000	14.0000
65.0000	242.6667	2.0000	0.0208	10.0000	10.0000
66.0000	246.4000	6.0000	0.0125	6.0000	6.0000
67.0000	250.1333	10.0000	0.0042	2.0000	2.0000

68.0000	253.8667	13.0000	0.0271	13.0000	13.0000
69.0000	257.6000	1.0000	0.0188	9.0000	9.0000
70.0000	261.3333	5.0000	0.0104	5.0000	5.0000
71.0000	265.0667	9.0000	0.0021	1.0000	1.0000
72.0000	268.8000	12.0000	0.0250	12.0000	12.0000
73.0000	272.5333	0	0.0167	8.0000	8.0000
74.0000	276.2667	4.0000	0.0083	4.0000	4.0000
75.0000	280.0000	8.0000	0	0	0
76.0000	283.7333	11.0000	0.0229	11.0000	11.0000
77.0000	287.4667	15.0000	0.0146	7.0000	7.0000
78.0000	291.2000	3.0000	0.0062	3.0000	3.0000
79.0000	294.9333	6.0000	0.0292	14.0000	14.0000
80.0000	298.6667	10.0000	0.0208	10.0000	10.0000
81.0000	302.4000	14.0000	0.0125	6.0000	6.0000
82.0000	306.1333	2.0000	0.0042	2.0000	2.0000
83.0000	309.8667	5.0000	0.0271	13.0000	13.0000
84.0000	313.6000	9.0000	0.0188	9.0000	9.0000
85.0000	317.3333	13.0000	0.0104	5.0000	5.0000
86.0000	321.0667	1.0000	0.0021	1.0000	1.0000
87.0000	324.8000	4.0000	0.0250	12.0000	12.0000
88.0000	328.5333	8.0000	0.0167	8.0000	8.0000
89.0000	332.2667	12.0000	0.0083	4.0000	4.0000
90.0000	336.0000	0	0	0	0
91.0000	339.7333	3.0000	0.0229	11.0000	11.0000
92.0000	343.4667	7.0000	0.0146	7.0000	7.0000
93.0000	347.2000	11.0000	0.0062	3.0000	3.0000
94.0000	350.9333	14.0000	0.0292	14.0000	14.0000
95.0000	354.6667	2.0000	0.0208	10.0000	10.0000
96.0000	358.4000	6.0000	0.0125	6.0000	6.0000
97.0000	362.1333	10.0000	0.0042	2.0000	2.0000
98.0000	365.8667	13.0000	0.0271	13.0000	13.0000
99.0000	369.6000	1.0000	0.0188	9.0000	9.0000
100.0000	373.3333	5.0000	0.0104	5.0000	5.0000
101.0000	377.0667	9.0000	0.0021	1.0000	1.0000
102.0000	380.8000	12.0000	0.0250	12.0000	12.0000
103.0000	384.5333	0	0.0167	8.0000	8.0000
104.0000	388.2667	4.0000	0.0083	4.0000	4.0000
105.0000	392.0000	8.0000	0	0	0
106.0000	395.7333	11.0000	0.0229	11.0000	11.0000
107.0000	399.4667	15.0000	0.0146	7.0000	7.0000
108.0000	403.2000	3.0000	0.0062	3.0000	3.0000
109.0000	406.9333	6.0000	0.0292	14.0000	14.0000
110.0000	410.6667	10.0000	0.0208	10.0000	10.0000
111.0000	414.4000	14.0000	0.0125	6.0000	6.0000
112.0000	418.1333	2.0000	0.0042	2.0000	2.0000
113.0000	421.8667	5.0000	0.0271	13.0000	13.0000
114.0000	425.6000	9.0000	0.0188	9.0000	9.0000
115.0000	429.3333	13.0000	0.0104	5.0000	5.0000
116.0000	433.0667	1.0000	0.0021	1.0000	1.0000
117.0000	436.8000	4.0000	0.0250	12.0000	12.0000
118.0000	440.5333	8.0000	0.0167	8.0000	8.0000
119.0000	444.2667	12.0000	0.0083	4.0000	4.0000
120.0000	448.0000	0	0	0	0
121.0000	451.7333	3.0000	0.0229	11.0000	11.0000
122.0000	455.4667	7.0000	0.0146	7.0000	7.0000
123.0000	459.2000	11.0000	0.0062	3.0000	3.0000
124.0000	462.9333	14.0000	0.0292	14.0000	14.0000
125.0000	466.6667	2.0000	0.0208	10.0000	10.0000
126.0000	470.4000	6.0000	0.0125	6.0000	6.0000
127.0000	474.1333	10.0000	0.0042	2.0000	2.0000
128.0000	477.8667	13.0000	0.0271	13.0000	13.0000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Time Interval in Tics
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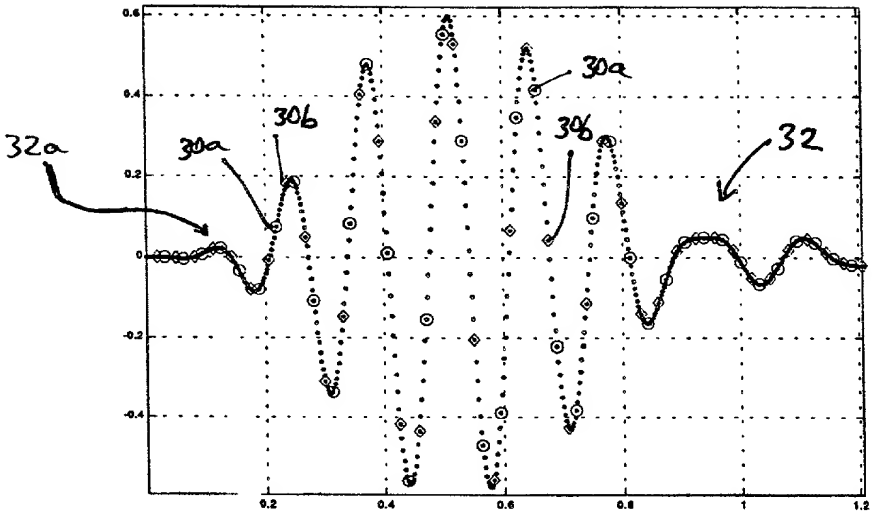
16 14
24
Transmit Clock
(32 mHz)
Phase Corr. Mod.
14
Table Address
Table Select
Pulse Shape Table 0
Pulse Shape Table 1
Pulse Shape Table 14
MUX
18
15
Sample Value
DAC
LPF
Analog Pulse Waveform
20
22

Figure 1

Figure 2A



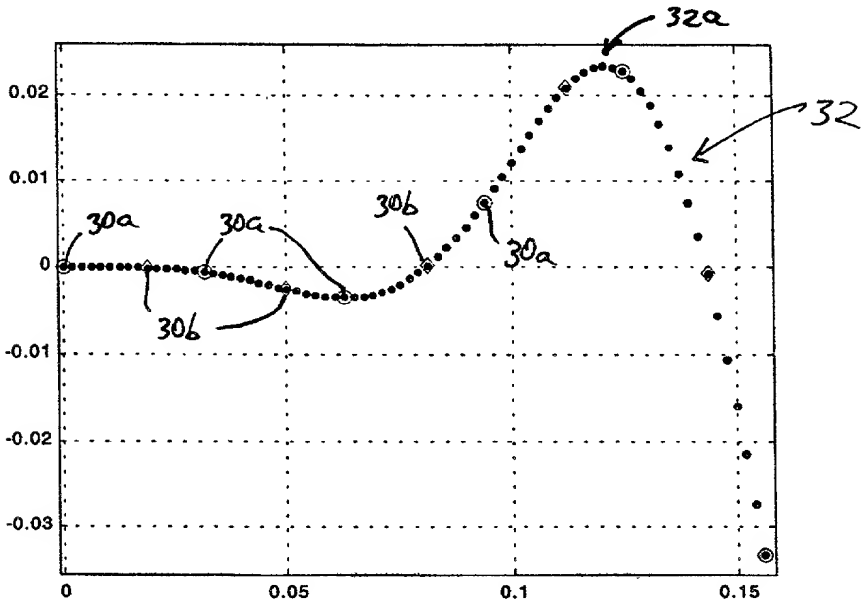


Figure 2B

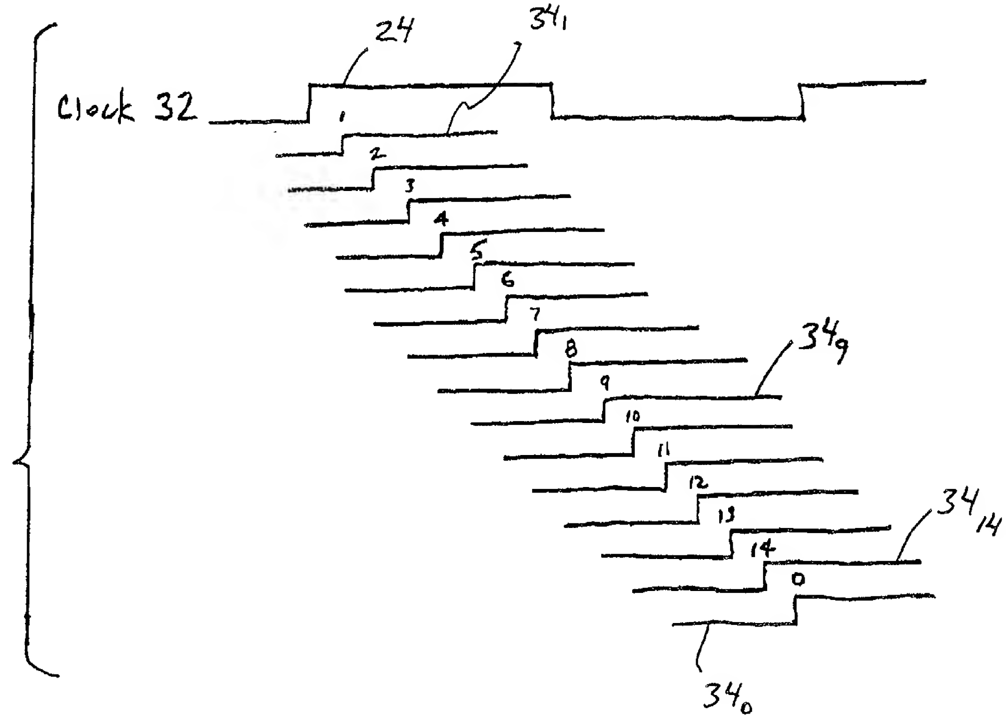


Figure 3

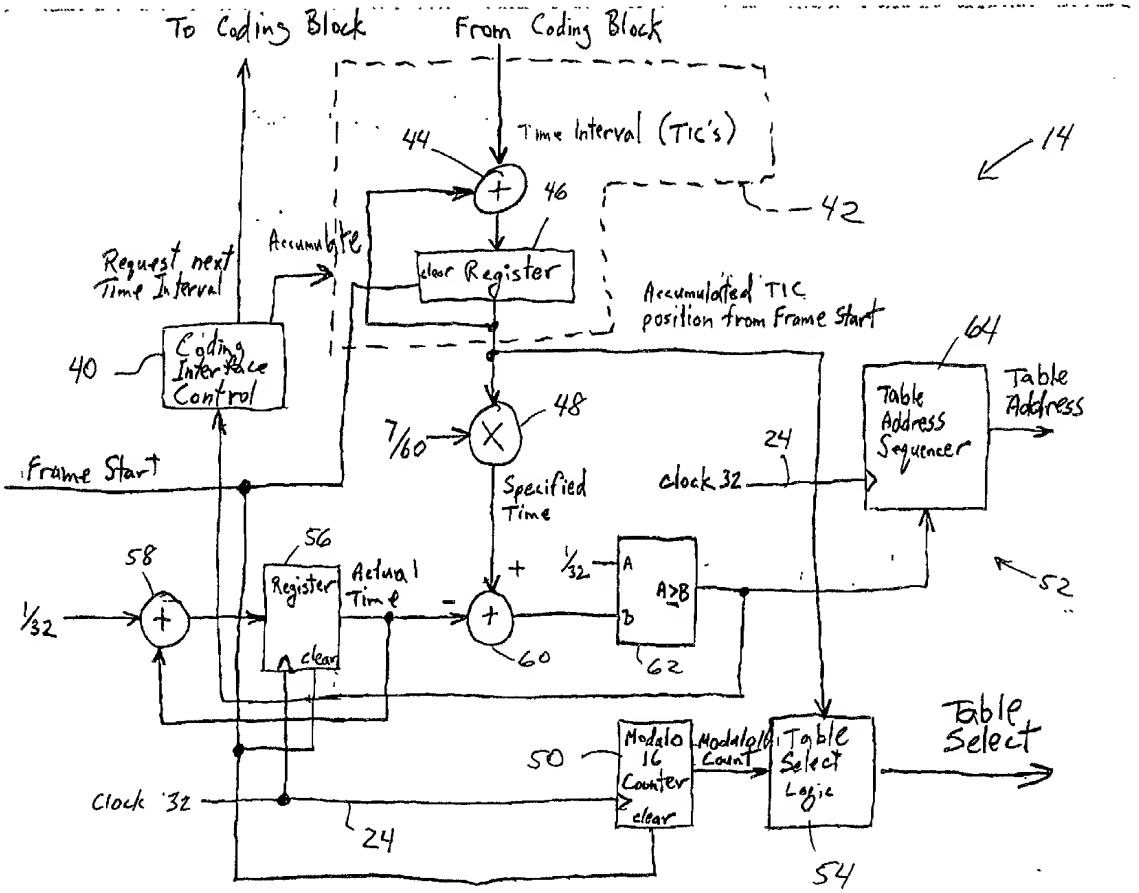


Figure 4

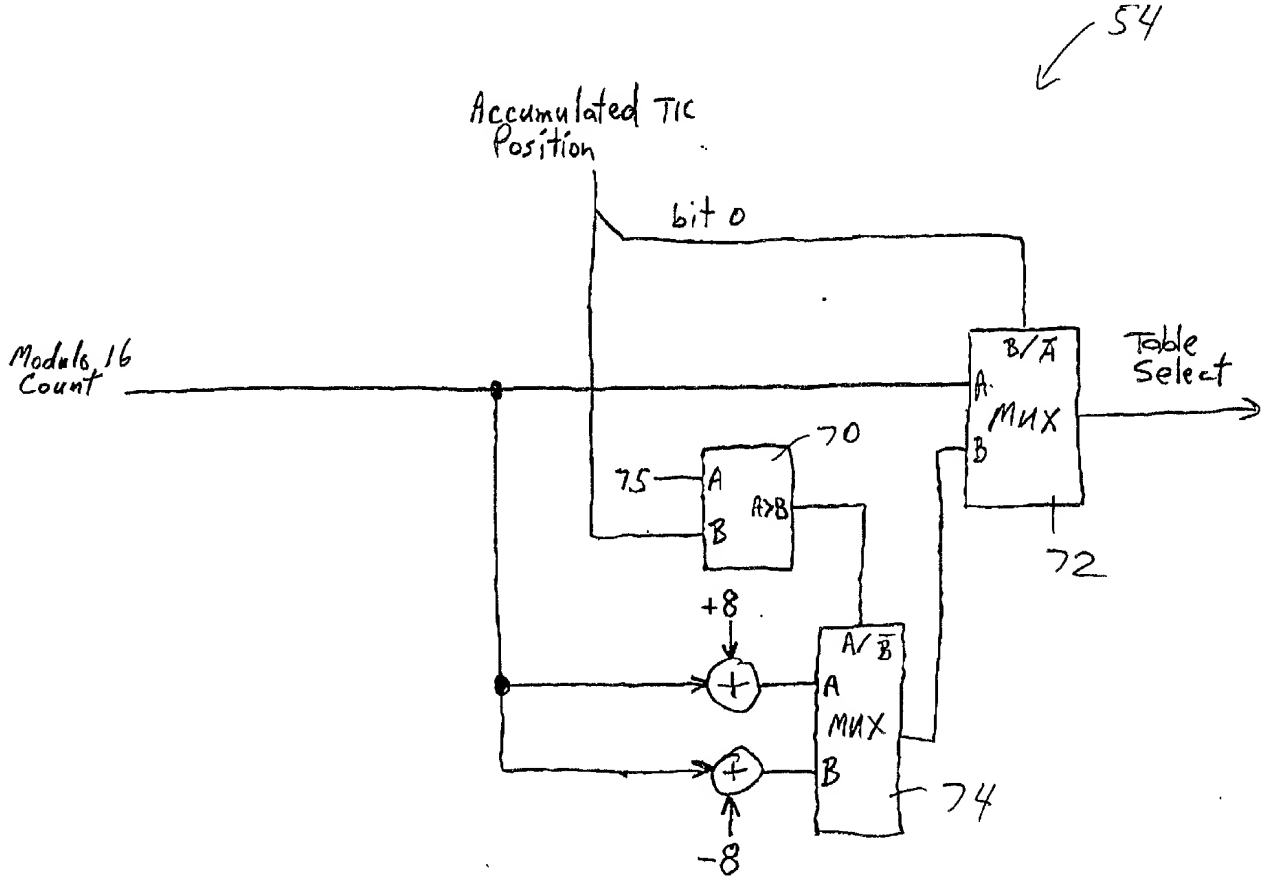
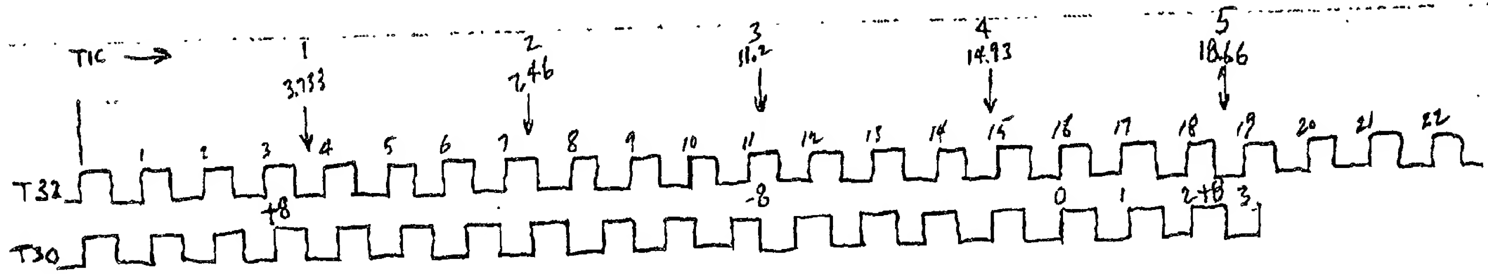


Figure 5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T30
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3
11.2
4
14.93
5
18.66
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
+8
-8
0 1 2 +8 3

Figure 6

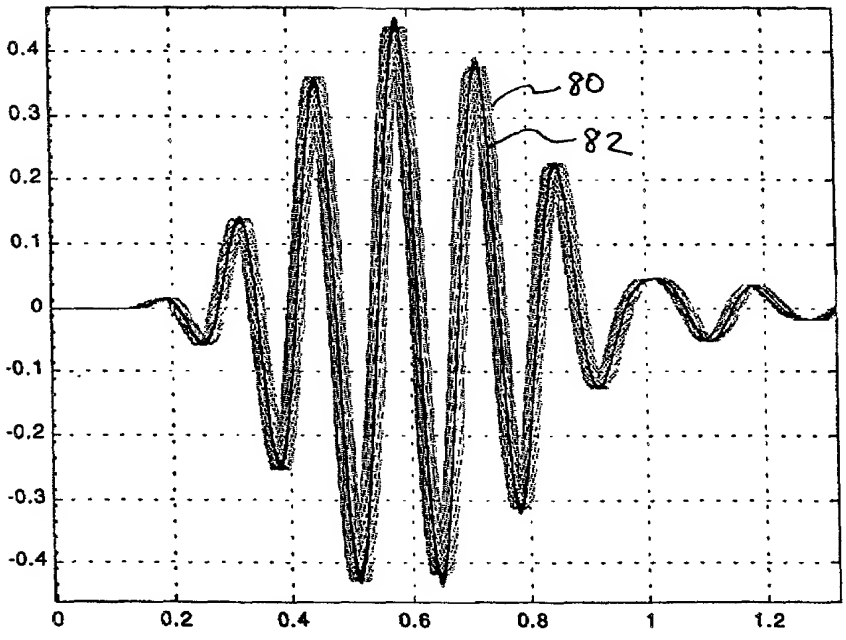

Figure 7

Docket No. 95-346

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought on the invention entitled **ARRANGEMENT FOR REDUCING TRANSMITTED JITTER**

[X] is attached hereto [ ] was filed on as Application Serial No. and was amended on (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known to me to be material to patentability in accordance with Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			Priority Claimed	
Number	Country	Day/Month/Year filed	Yes	No

I hereby claim the benefit under 35 USC §119(e) of any United States provisional application(s) listed below.

Prior Provisional Application(s):

Application Number	Filing Date
60/218,571	July 13, 2000

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U. S. Application(s):

Serial No.	Filing Date	Status: Patented, Pending, Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) and/or agent(s): Leon R. Turkevich, Reg. No. 34,035, and the attorneys of Customer No. 20736, all of:

FARKAS & MANELLI, PLLC
2000 M Street, N.W., 7th Floor
Washington, D.C. 20036-3307

and Richard J. Roddy, Reg. No. 27,688, William D. Zahrt II, Reg. No. 26,070, Paul S. Drake, Reg. No. 33,491, Louis A. Riley, Reg. No. 39,817; Elizabeth A. Apperley, Reg. No. 36,428; and Harry A. Wolin, Reg. No. 32,638, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and all future correspondence should be addressed to Customer No. 20736.

****

Full name of sole or first inventor: Colin D. Nayler

Inventor's signature: Colin D Nayler Date: 8-1-00

Residence: 691 Ontario Ct., Apt. 7, Sunnyvale, CA 94087

Citizenship: USA

Post Office Address: same as above